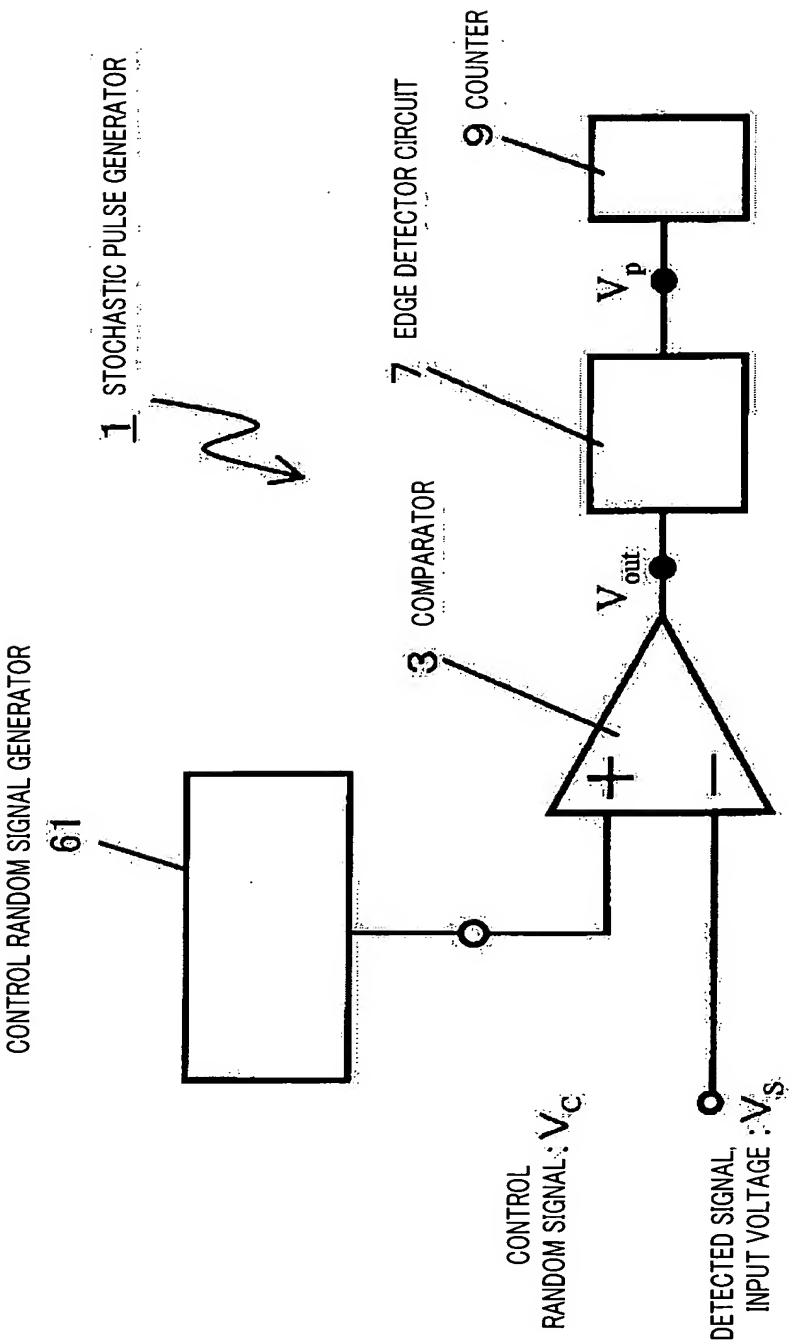


Fig. 1

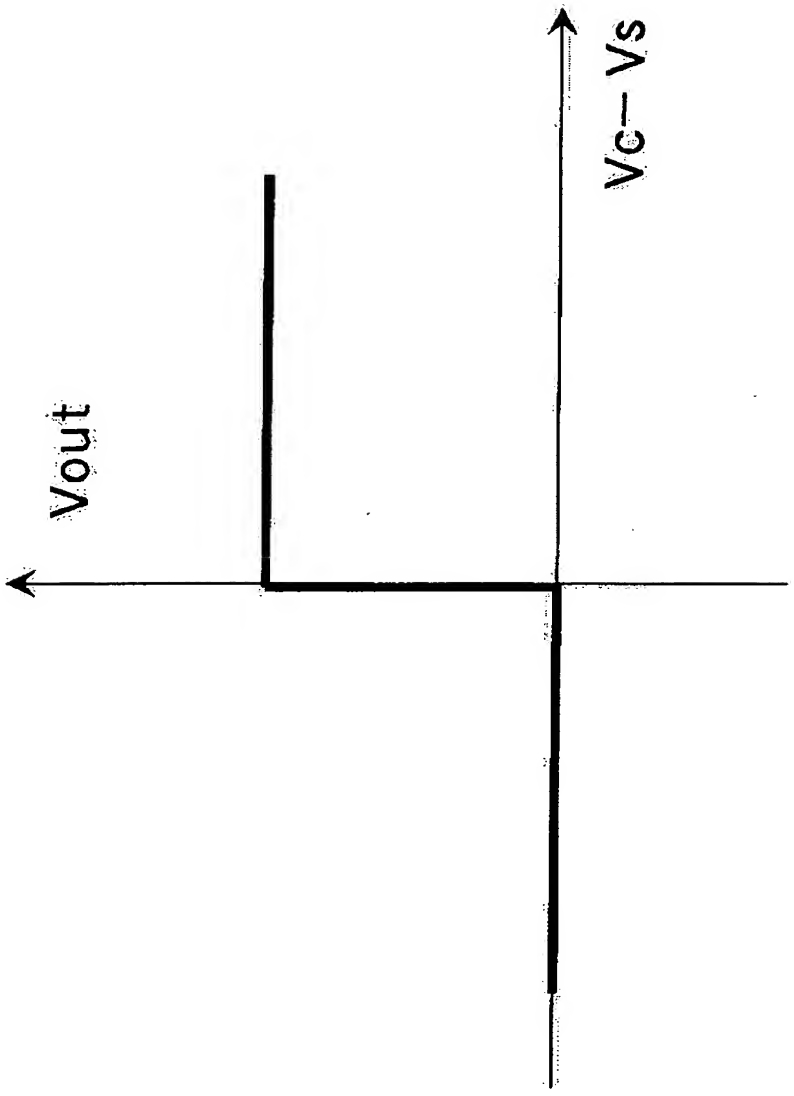


Fig. 2

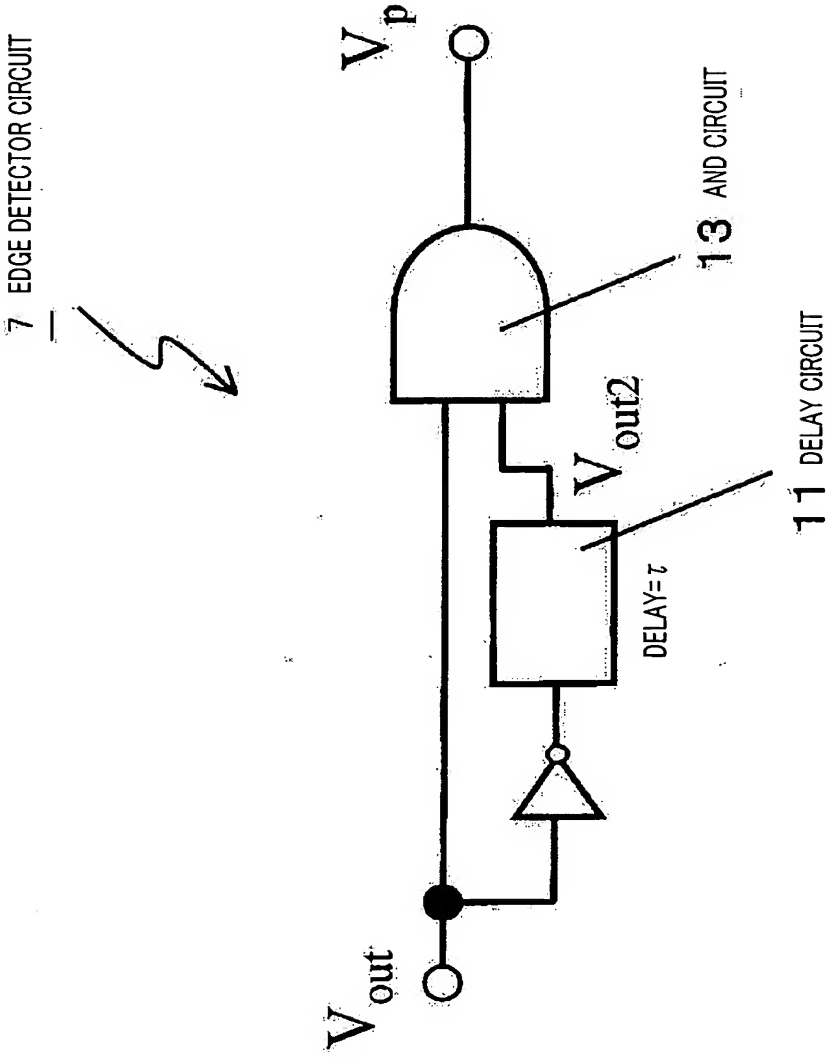

7 EDGE DETECTOR CIRCUIT
V_p
13 AND CIRCUIT
V_{out2}
11 DELAY CIRCUIT
DELAY= τ
V_{out}

Fig. 3

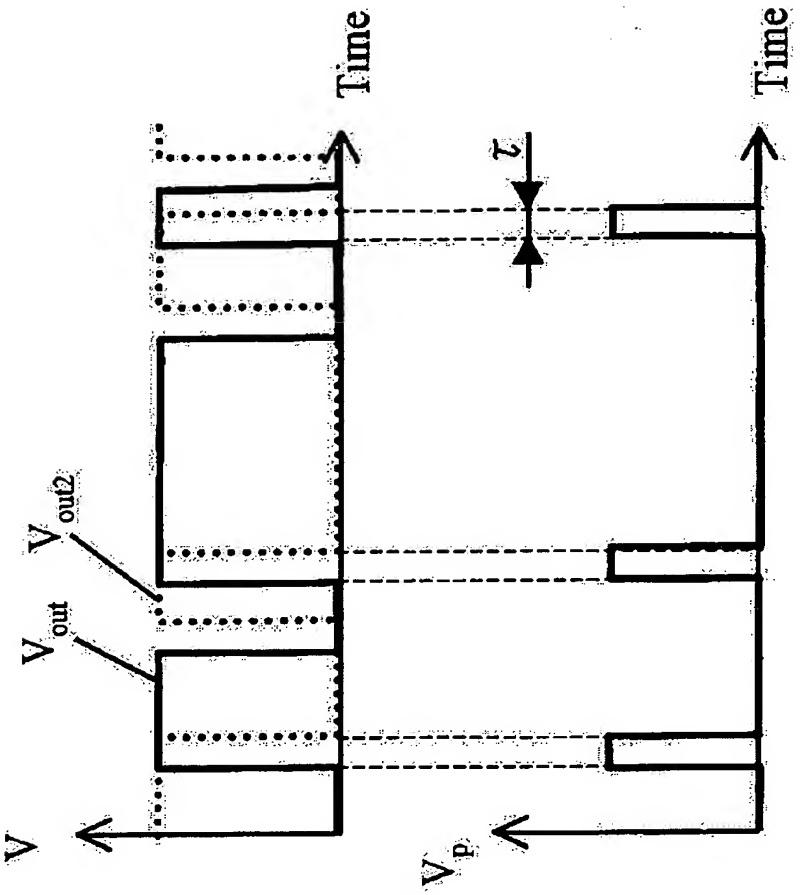


Fig. 4

Fig. 5(a)

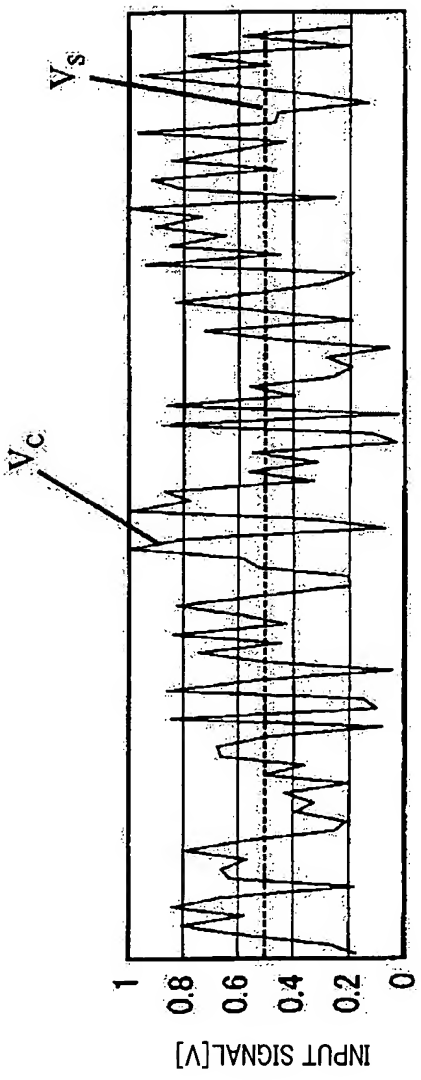
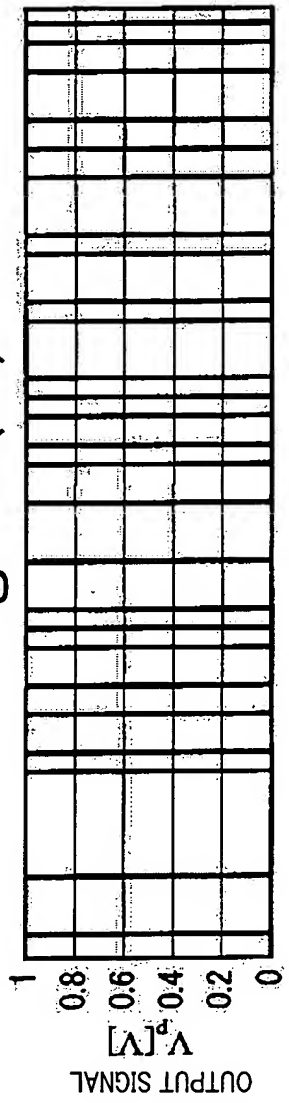

V_S
V_C
1
0.8
0.6
0.4
0.2
0
INPUT SIGNAL[V]

Fig. 5(b)


1
0.8
0.6
0.4
0.2
0
V_p[V]
OUTPUT SIGNAL

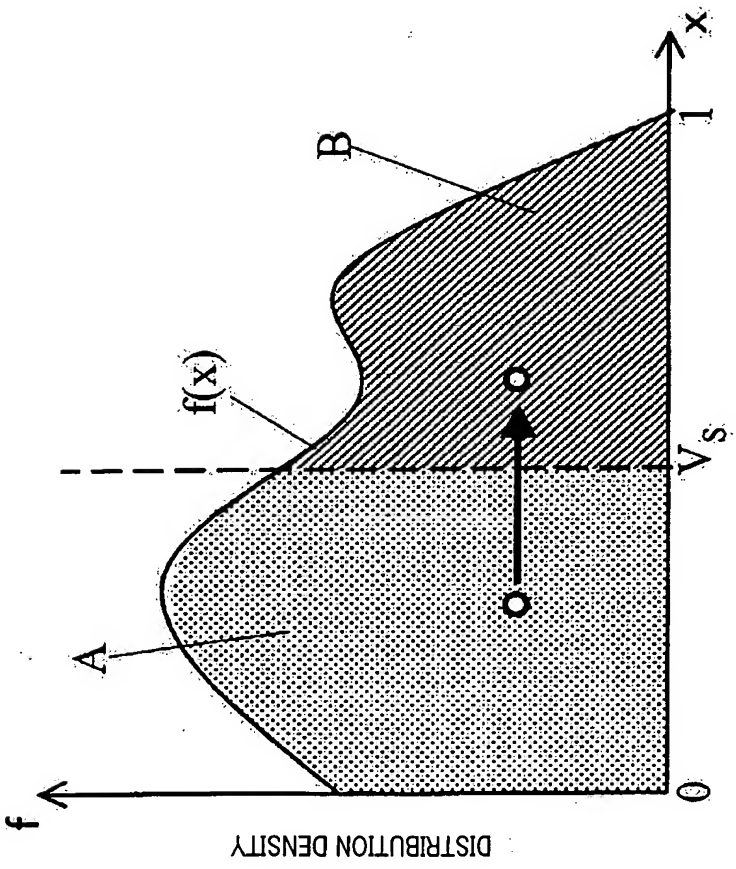


Fig. 6

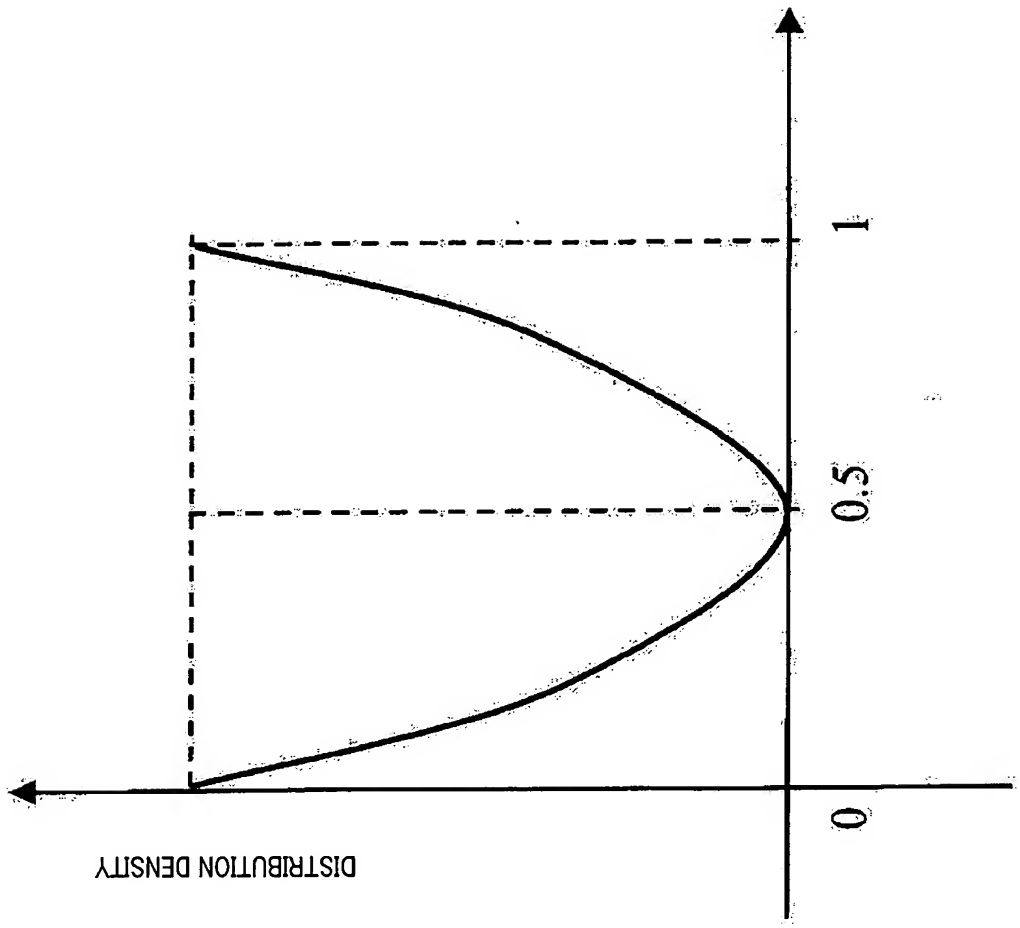


Fig. 7

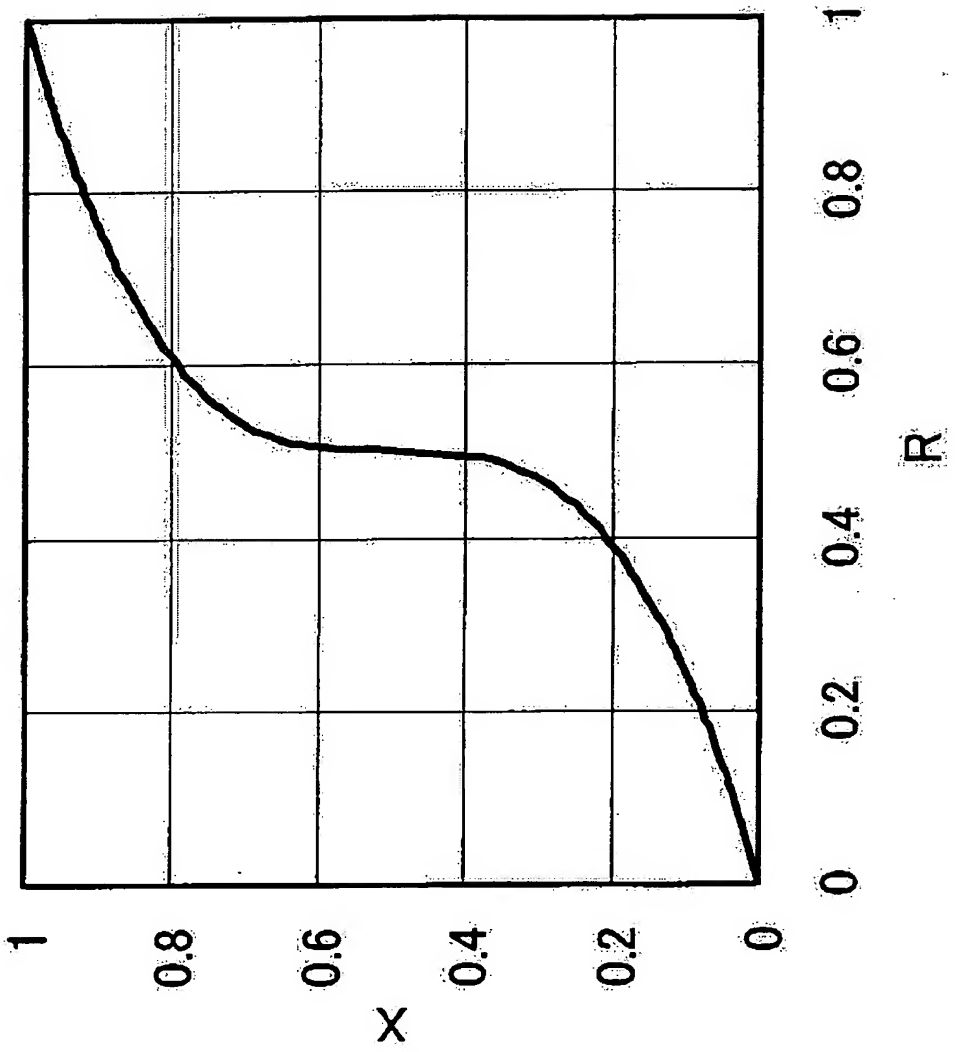


Fig. 8

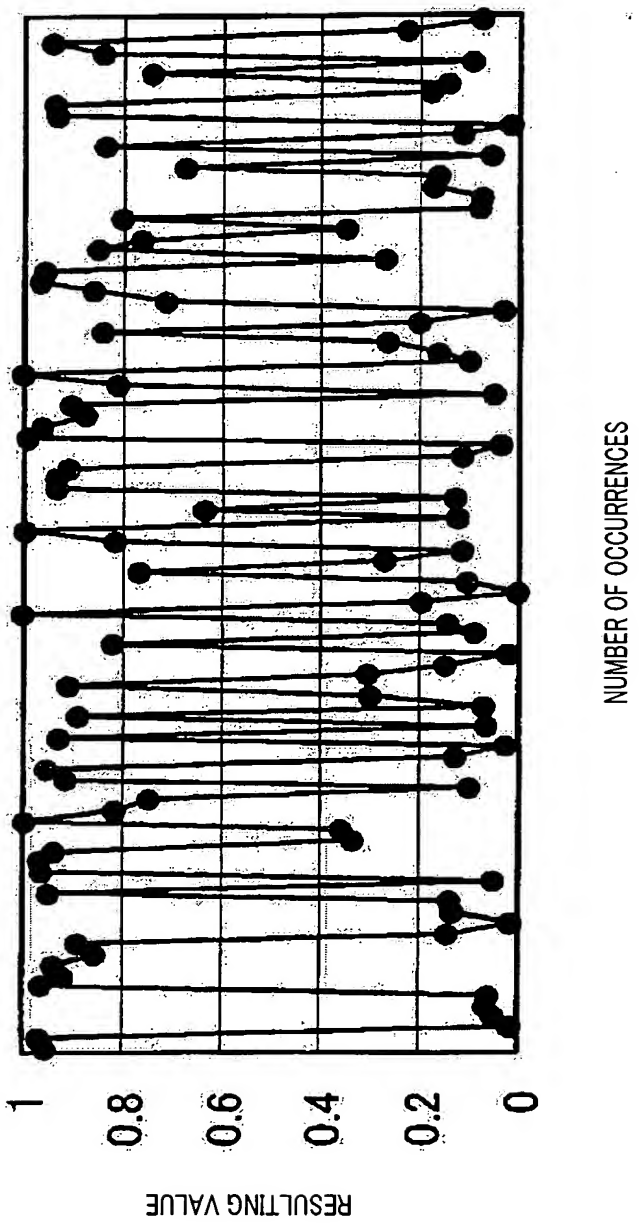


Fig. 9

Fig. 10(a)

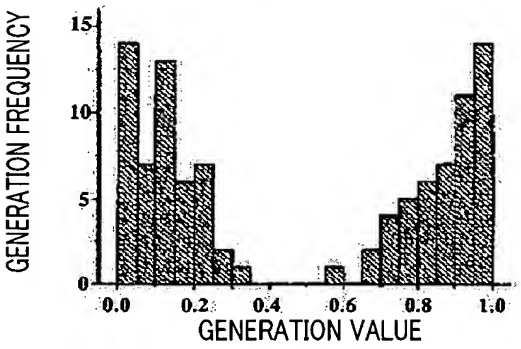


Fig. 10(b)

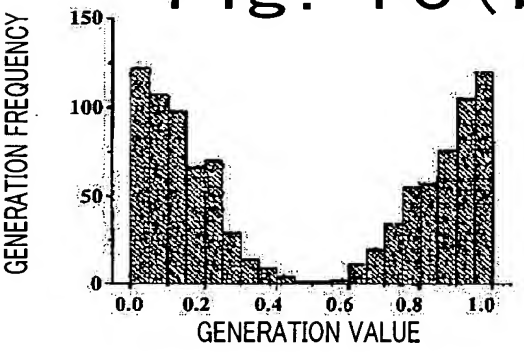
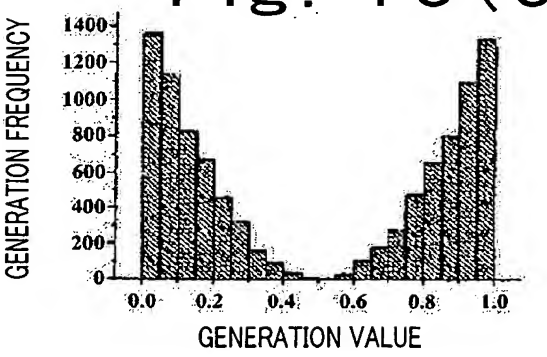


Fig. 10(c)



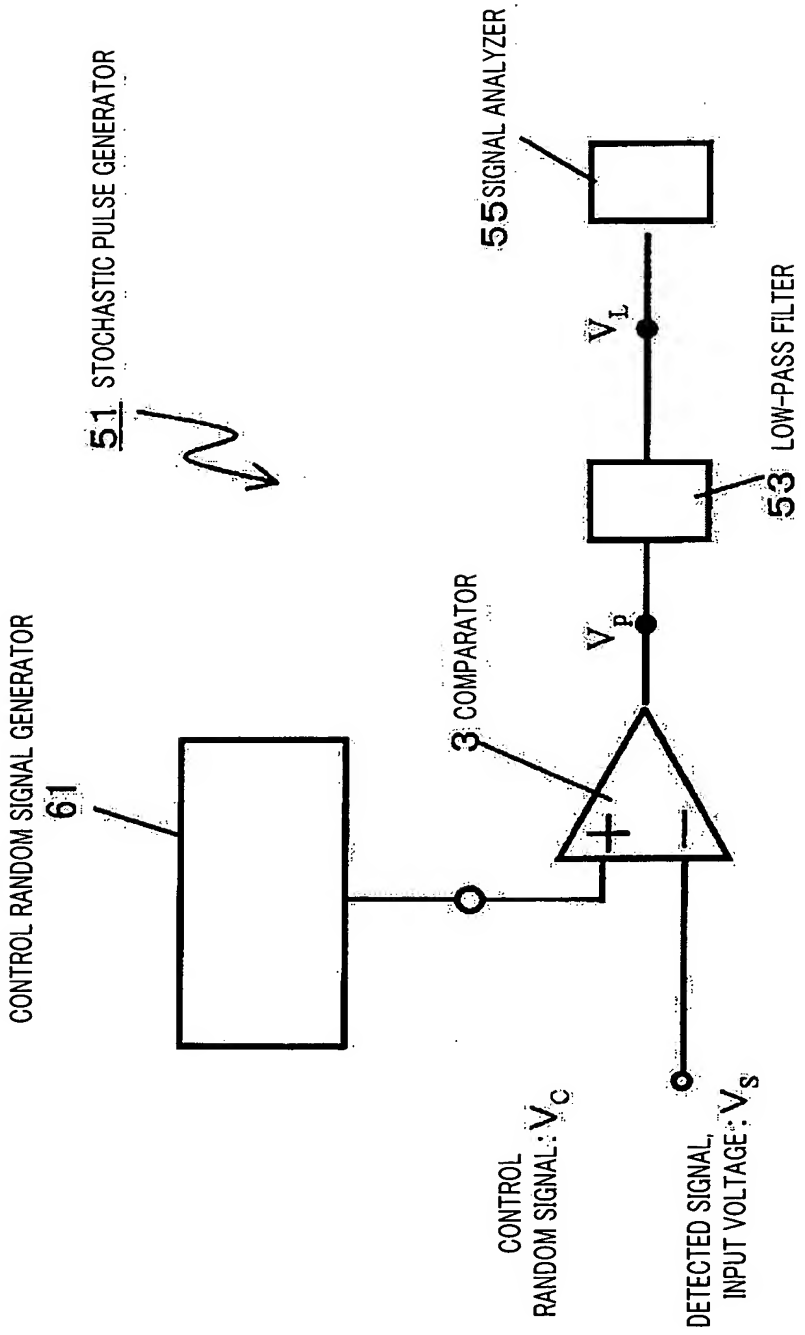

CONTROL RANDOM SIGNAL GENERATOR
61
51 STOCHASTIC PULSE GENERATOR
3 COMPARATOR
+
−
V_p
53 LOW-PASS FILTER
V_L
55 SIGNAL ANALYZER
CONTROL RANDOM SIGNAL: V_c
DETECTED SIGNAL, INPUT VOLTAGE: V_s

Fig. 11

Fig. 12(a)

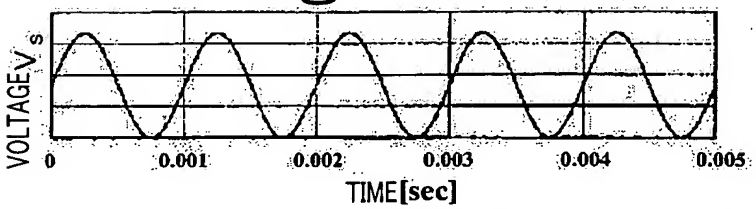


Fig. 12(b)

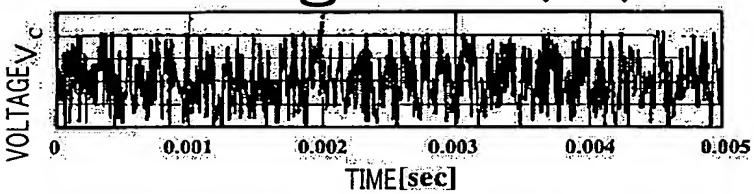


Fig. 12(c)

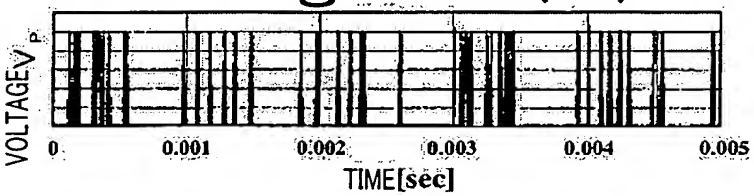


Fig. 12(d)

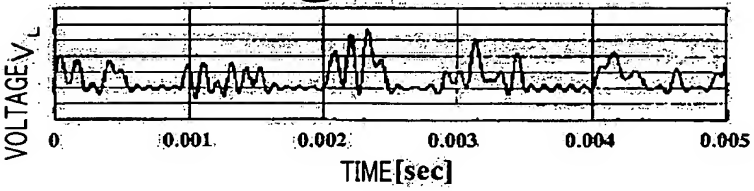
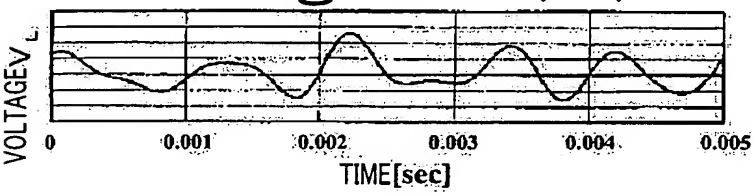


Fig. 12(e)



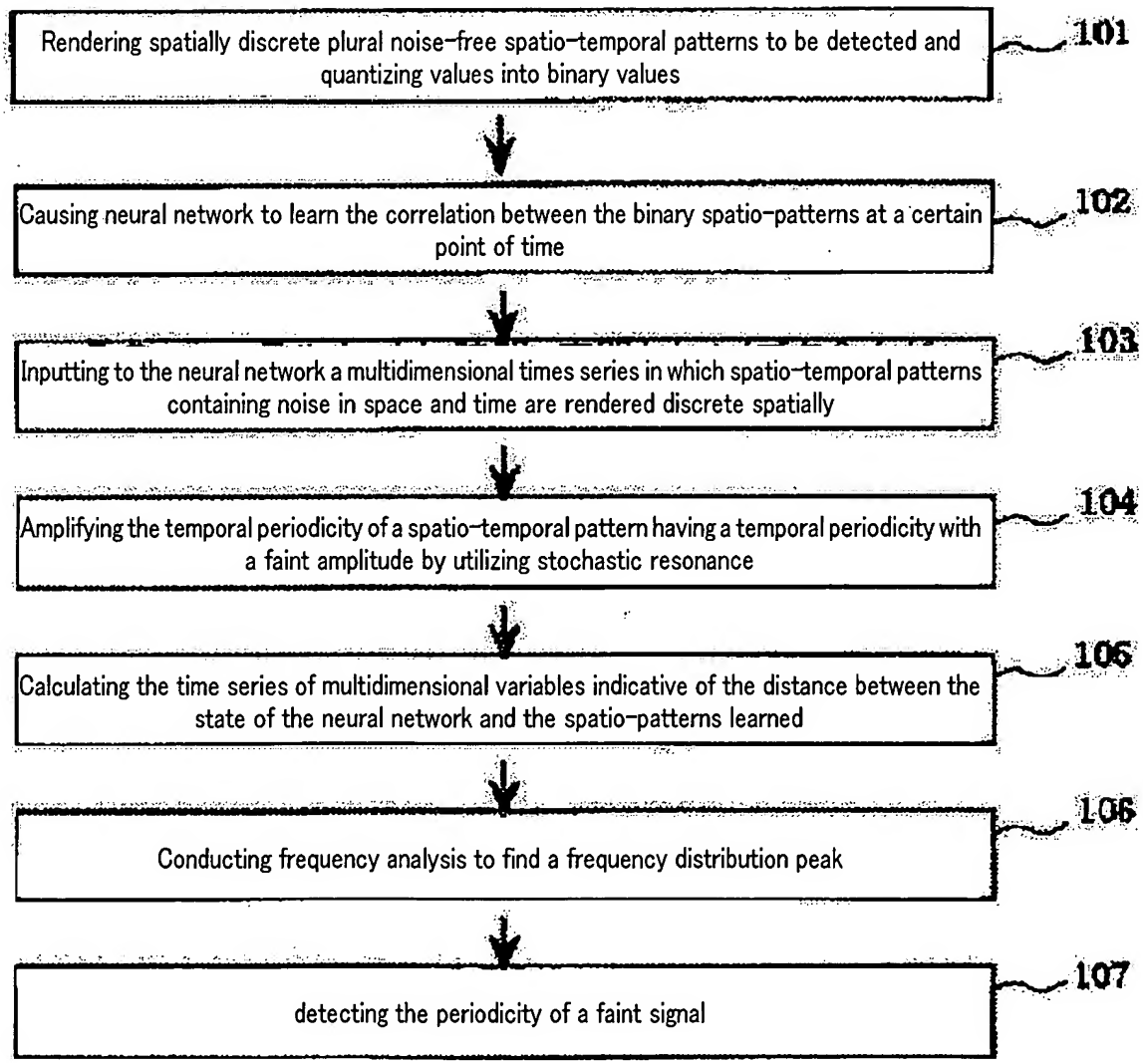

Rendering spatially discrete plural noise-free spatio-temporal patterns to be detected and quantizing values into binary values
101
Causing neural network to learn the correlation between the binary spatio-patterns at a certain point of time
102
Inputting to the neural network a multidimensional times series in which spatio-temporal patterns containing noise in space and time are rendered discrete spatially
103
Amplifying the temporal periodicity of a spatio-temporal pattern having a temporal periodicity with a faint amplitude by utilizing stochastic resonance
104
Calculating the time series of multidimensional variables indicative of the distance between the state of the neural network and the spatio-patterns learned
105
Conducting frequency analysis to find a frequency distribution peak
106
detecting the periodicity of a faint signal
107

Fig. 13

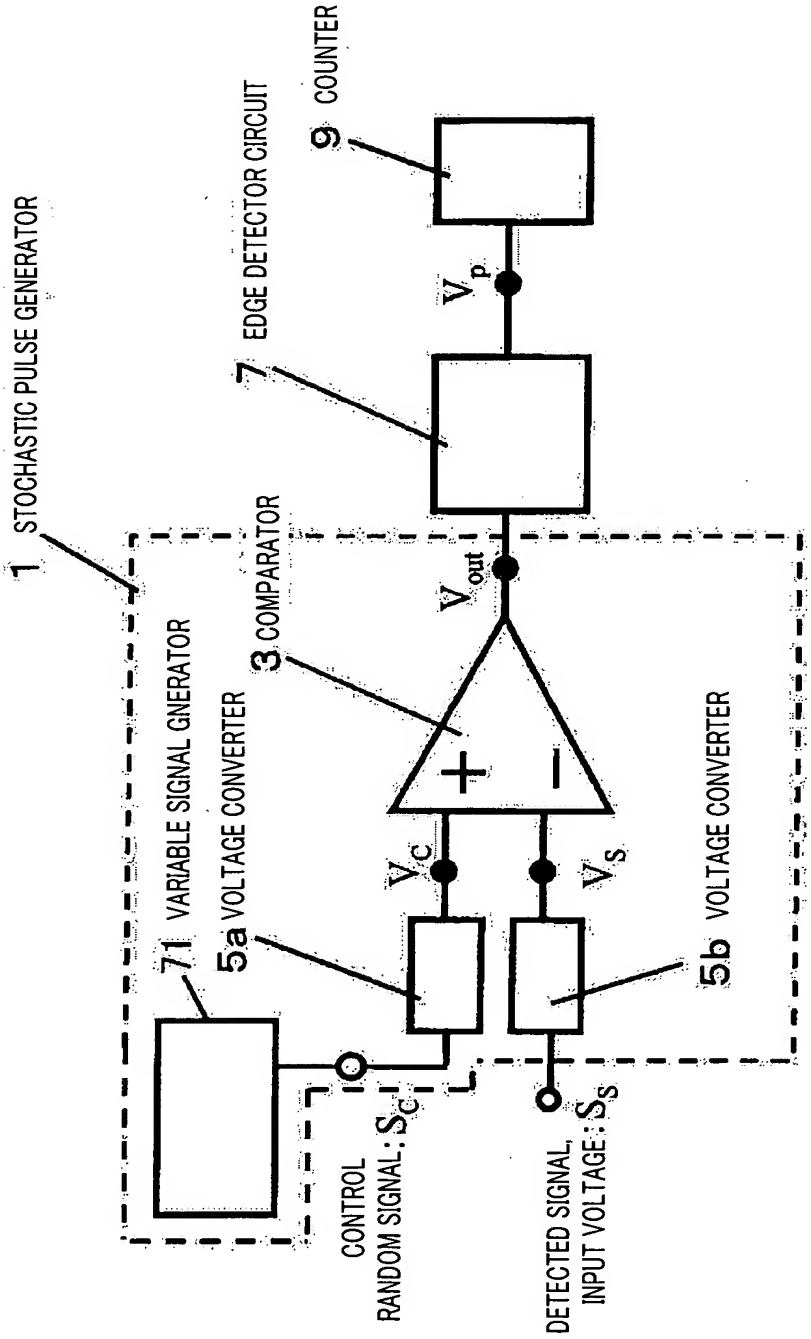

1 STOCHASTIC PULSE GENERATOR
71 VARIABLE SIGNAL GNERATOR
5a VOLTAGE CONVERTER
3 COMPARATOR
7 EDGE DETECTOR CIRCUIT
9 COUNTER
5b VOLTAGE CONVERTER
V_{out}
V_p
V_C
V_S
CONTROL RANDOM SIGNAL: S_C
DETECTED SIGNAL, INPUT VOLTAGE: S_S

Fig. 14

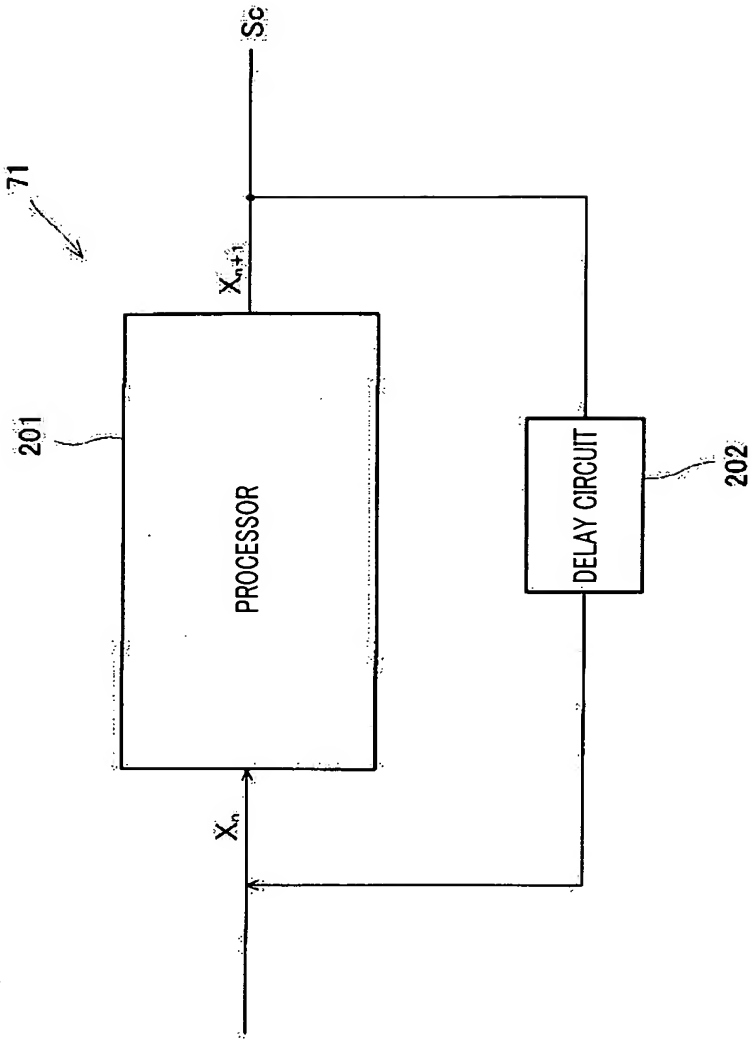


Fig. 15

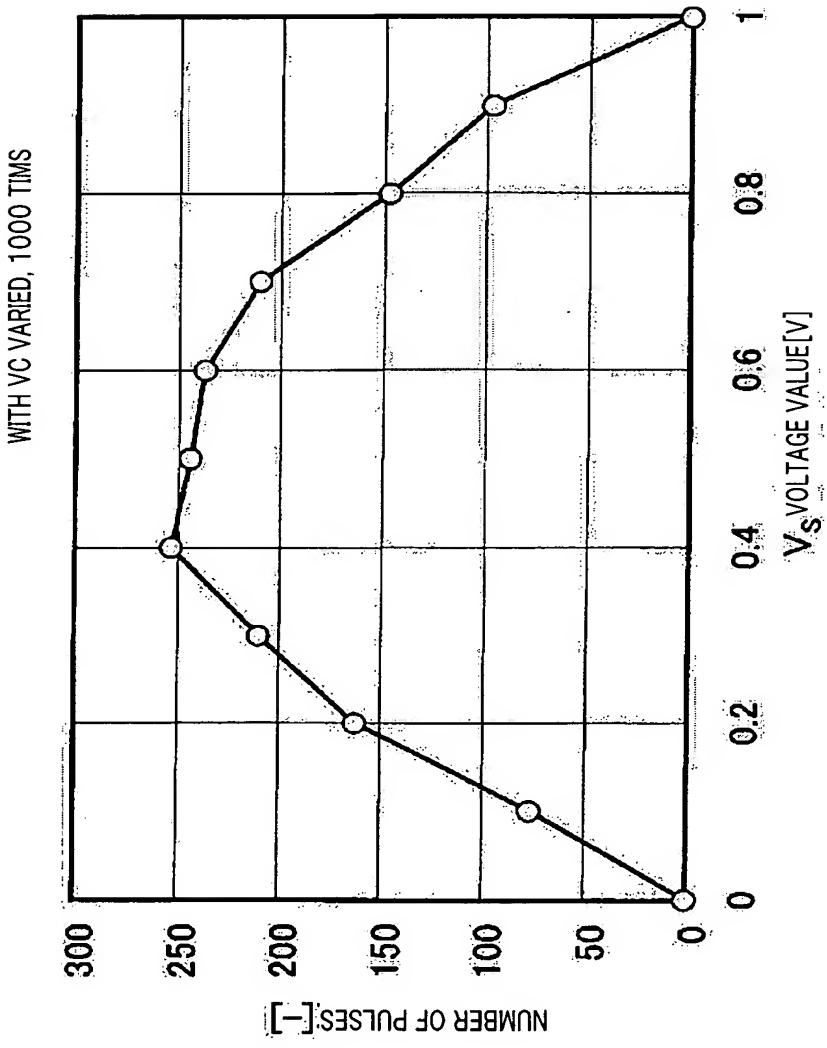

WITH VC VARIED, 1000 TIMS
NUMBER OF PULSES[—]
300
250
200
150
100
50
0
0
0.2
0.4
0.6
0.8
1
V_S VOLTAGE VALUE[V]

Fig. 16

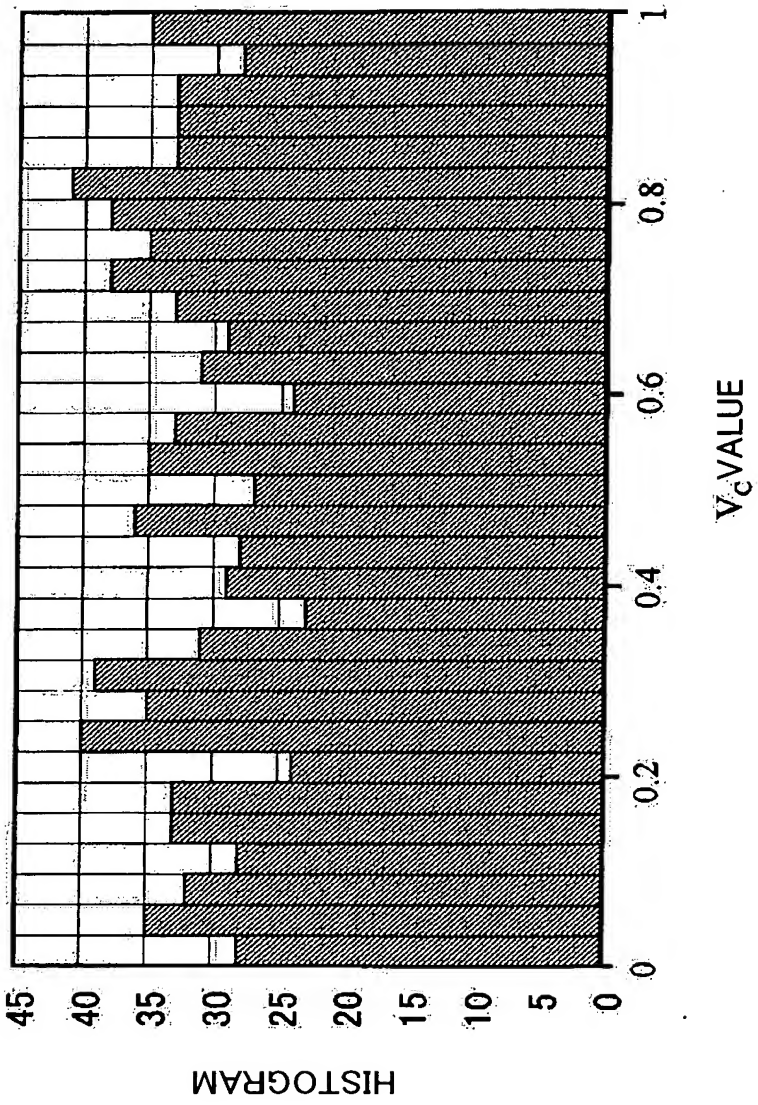


Fig. 17

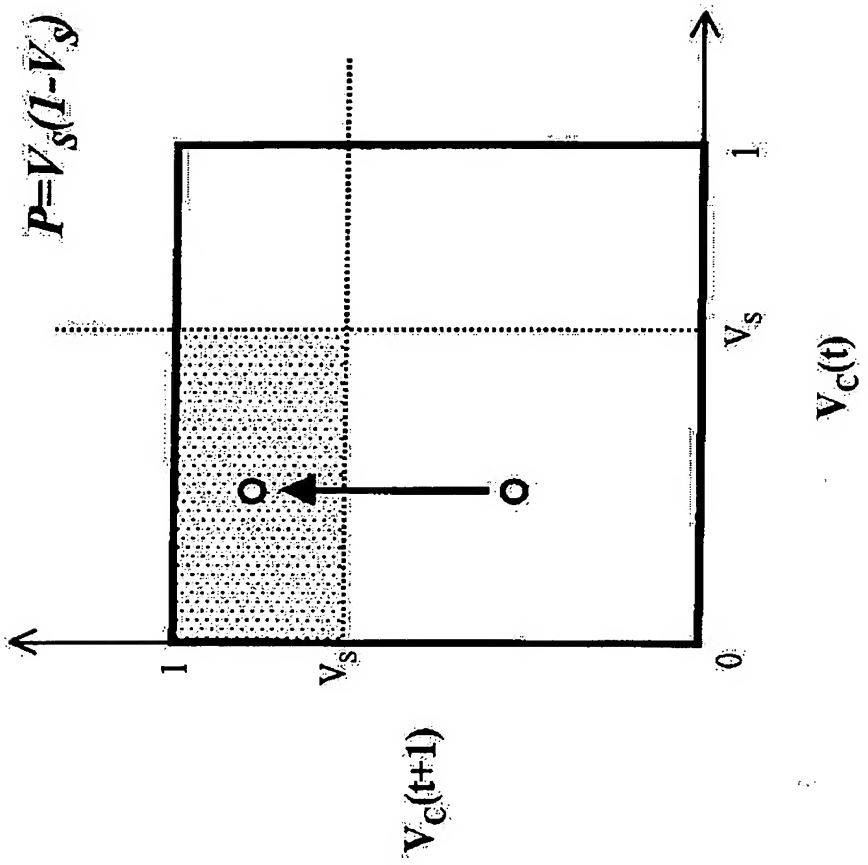


Fig. 18

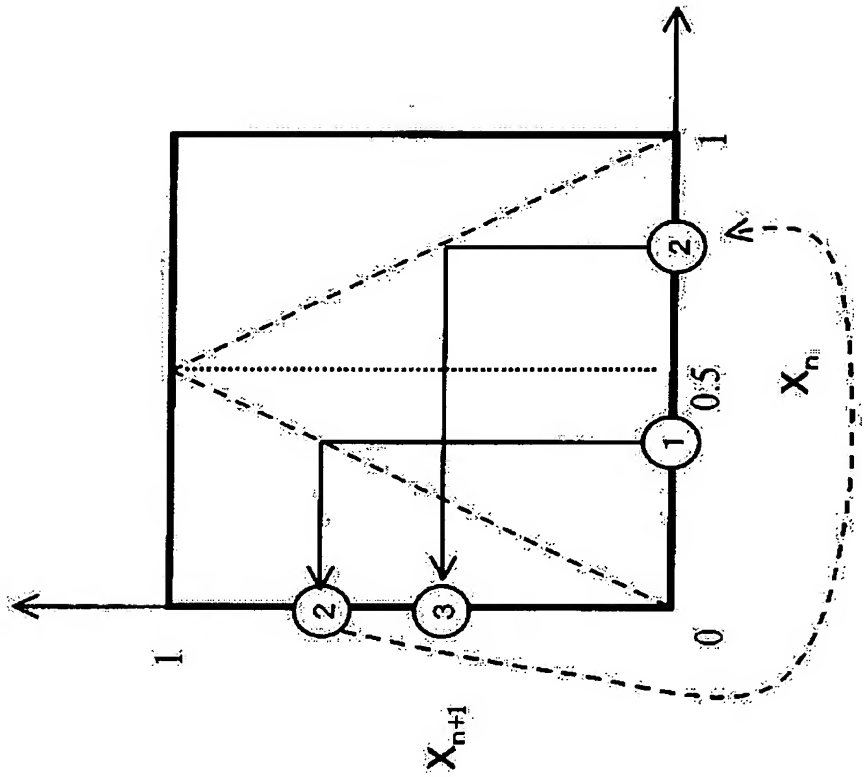


Fig. 19

Fig. 20(a) $V_S \leqq 2/3$

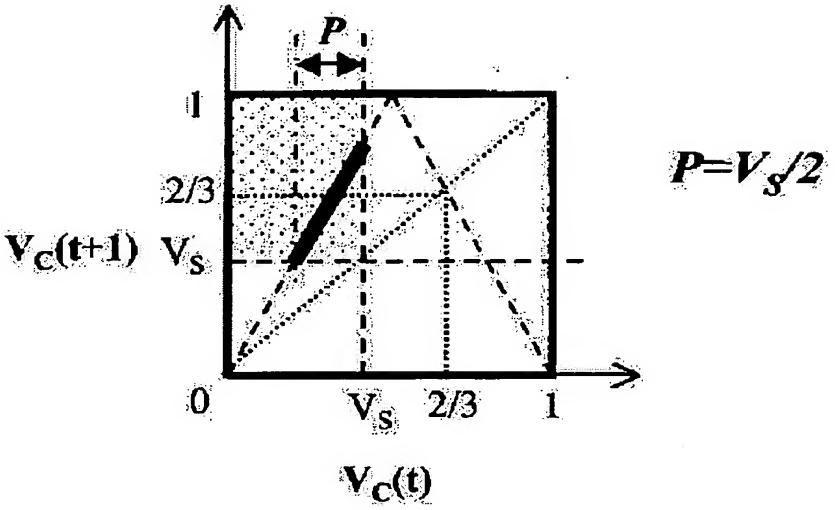
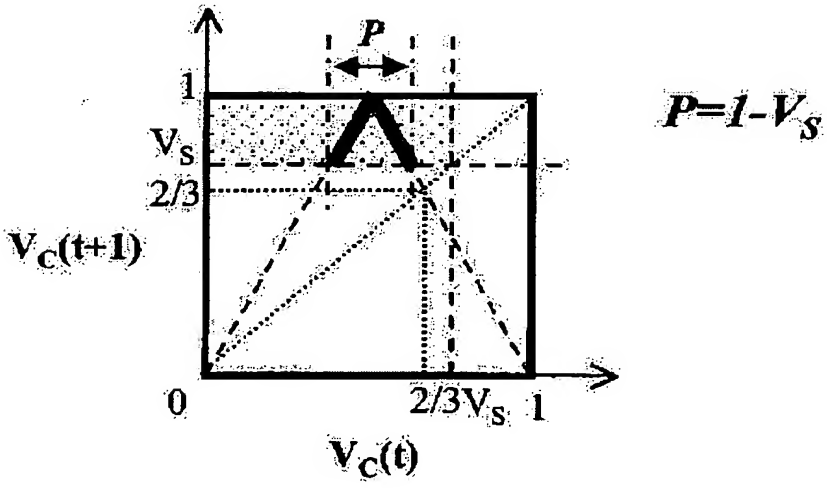


Fig. 20(b) $V_S \geqq 2/3$



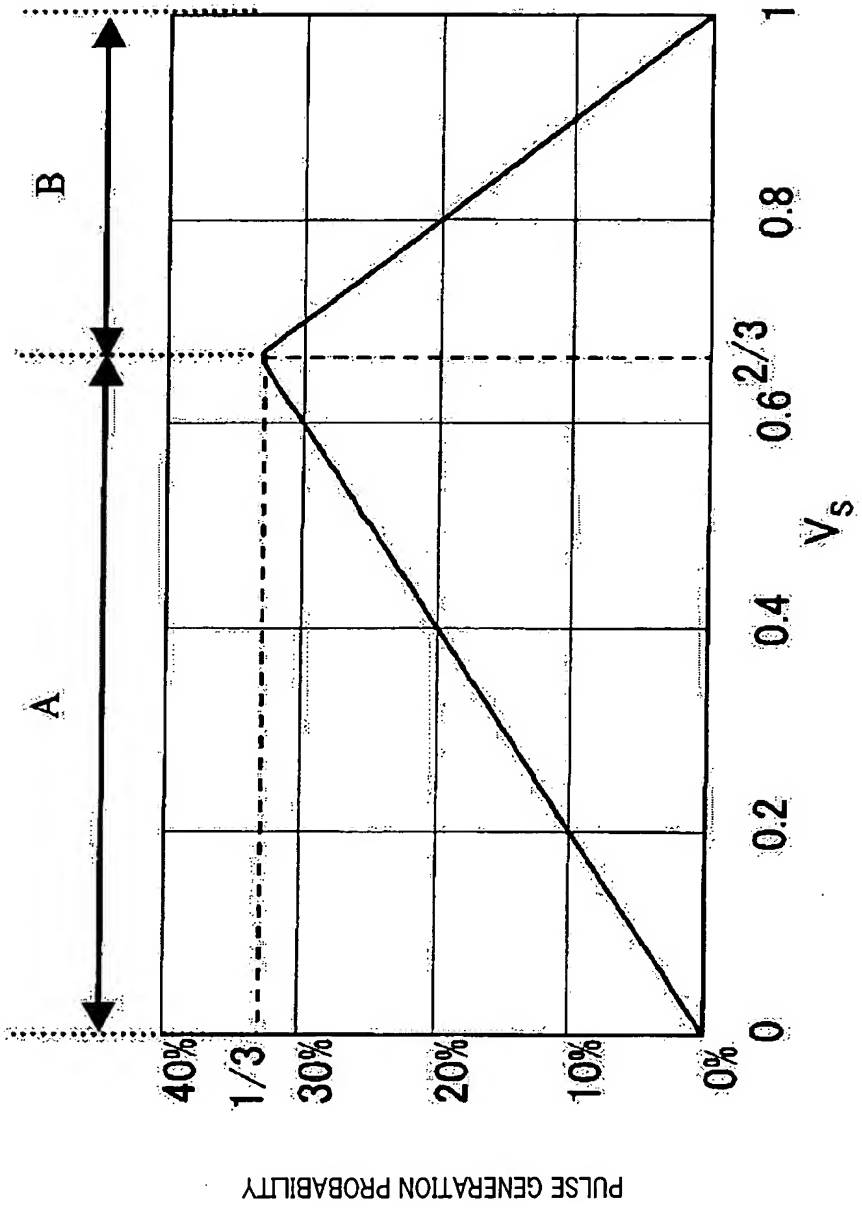

B
A
40%
1/3
30%
20%
10%
0%
0
0.2
0.4
0.6
2/3
0.8
1
V_S
PULSE GENERATION PROBABILITY

Fig. 21

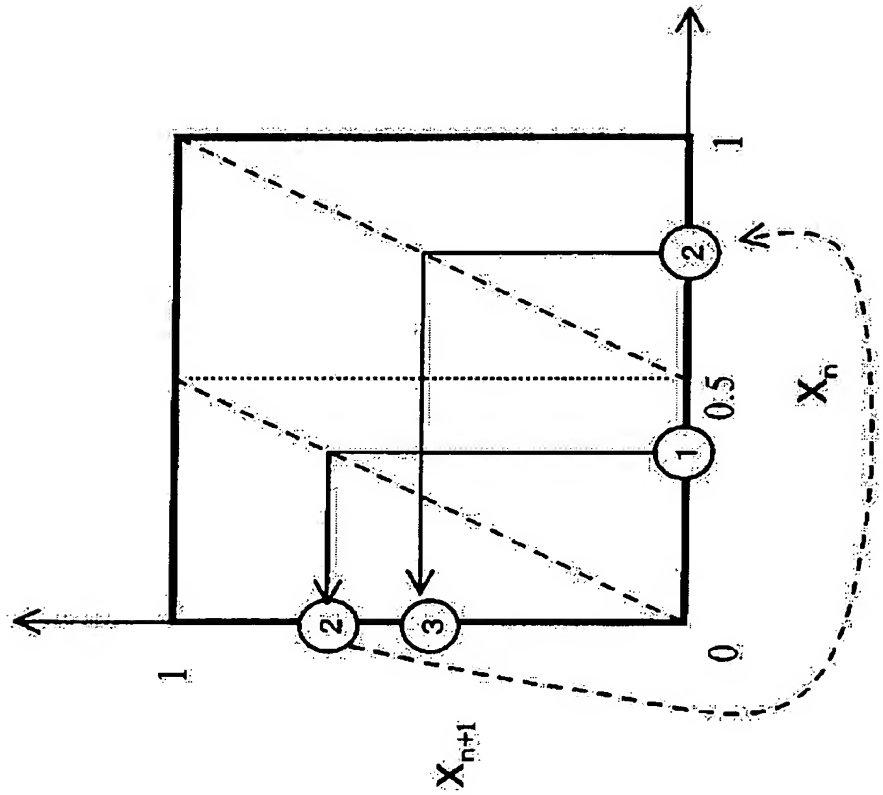
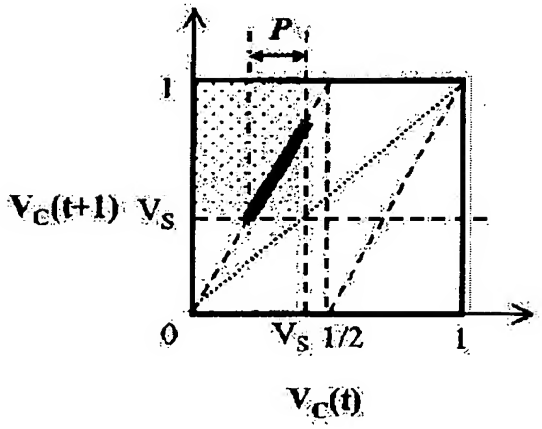


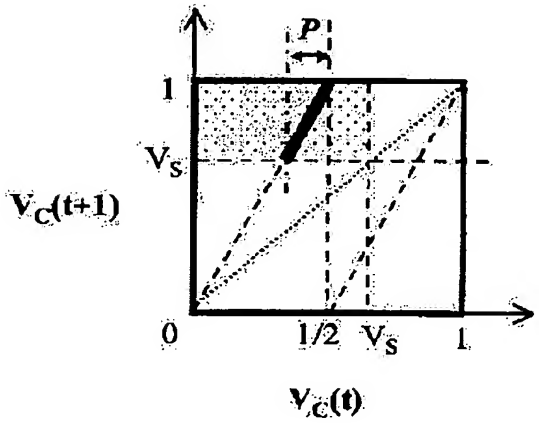
Fig. 22

Fig. 23(a) $V_S \leqq 1/2$



$P=V_S/2$

Fig. 23(b) $V_S \geqq 1/2$



$P=(1-V_S)/2$

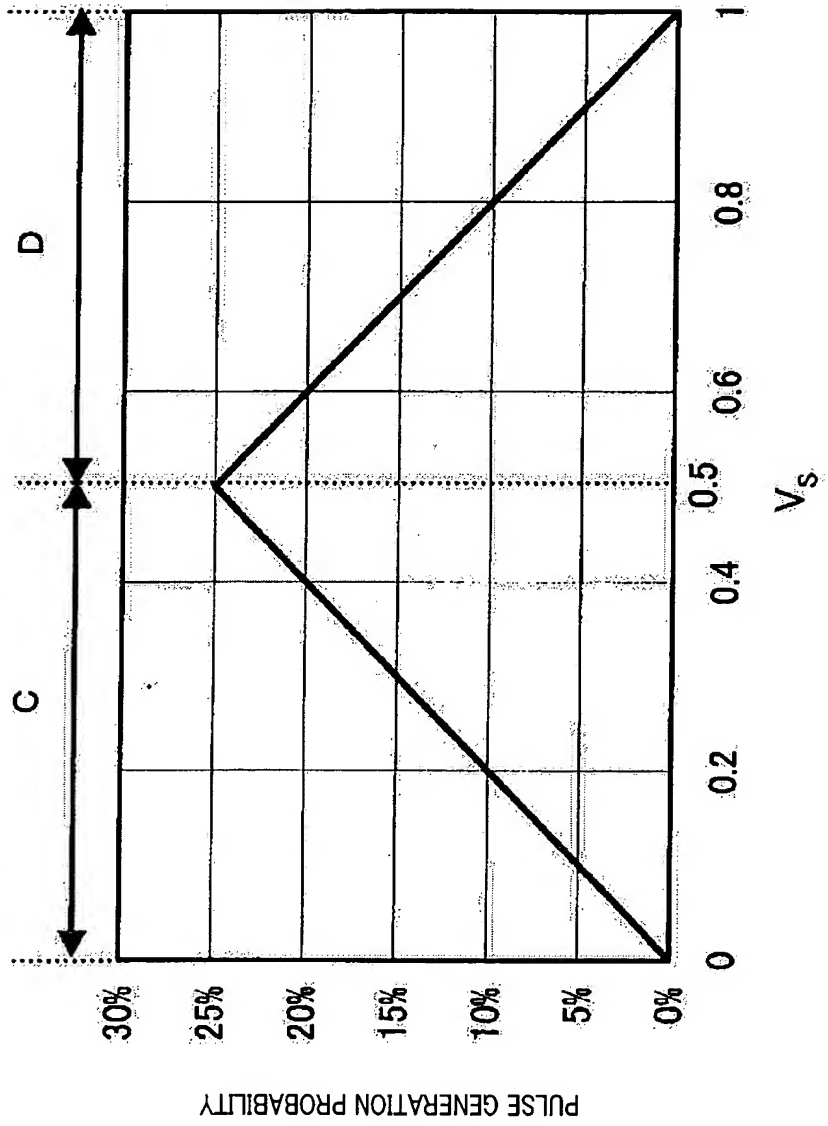

D
C
30%
25%
20%
15%
10%
5%
0%
0
0.2
0.4
0.5
0.6
0.8
1
V_S
PULSE GENERATION PROBABILITY

Fig. 24

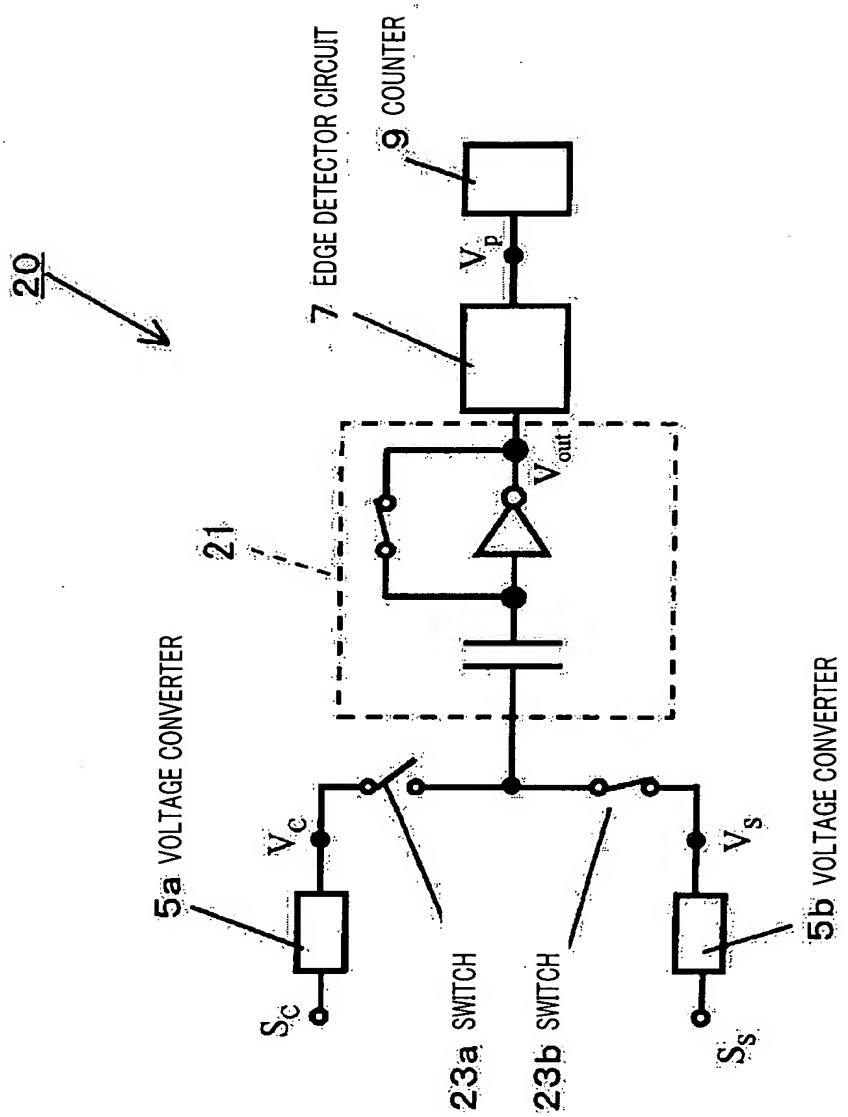

20
7 EDGE DETECTOR CIRCUIT
9 COUNTER
V_p
V_{out}
21
5a VOLTAGE CONVERTER
V_c
S_c
23a SWITCH
23b SWITCH
V_s
S_s
5b VOLTAGE CONVERTER

Fig. 25

Fig. 26(a) V_1 STORAGE

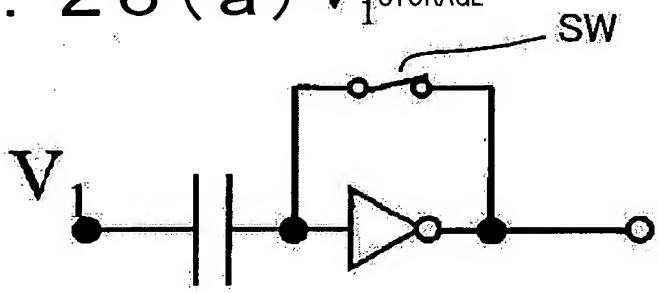


Fig. 26(b) COMPARISON

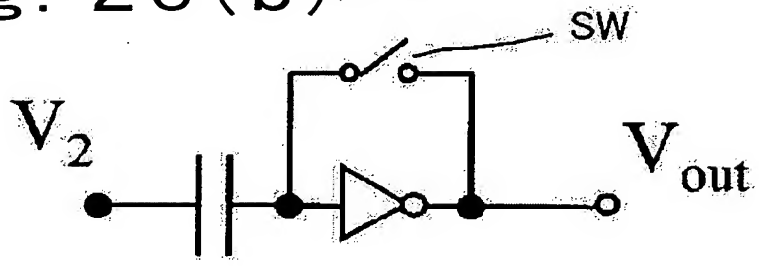


Fig. 27(a)

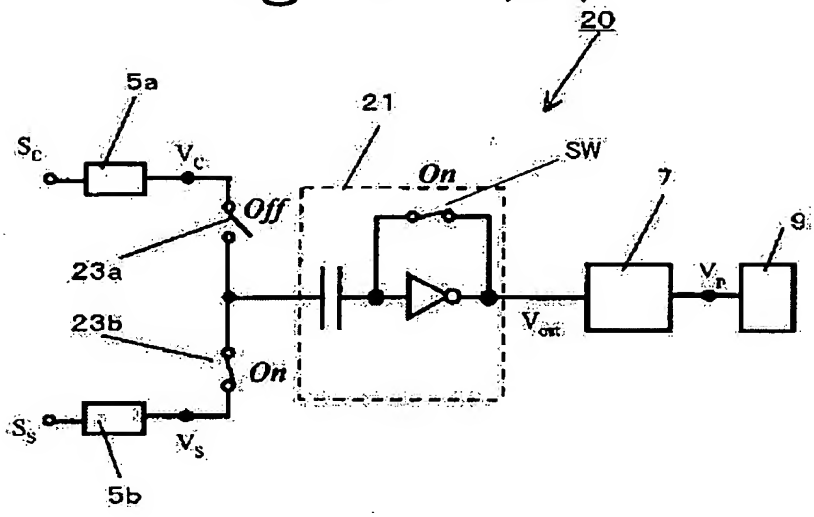
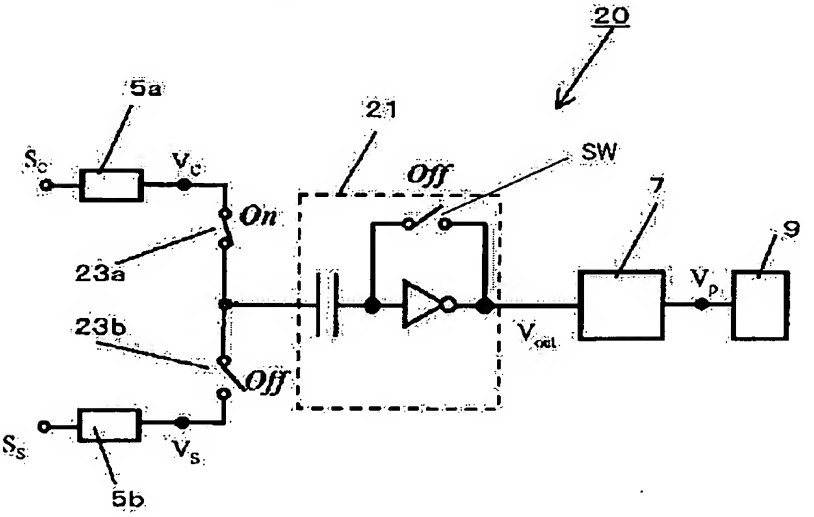


Fig. 27(b)



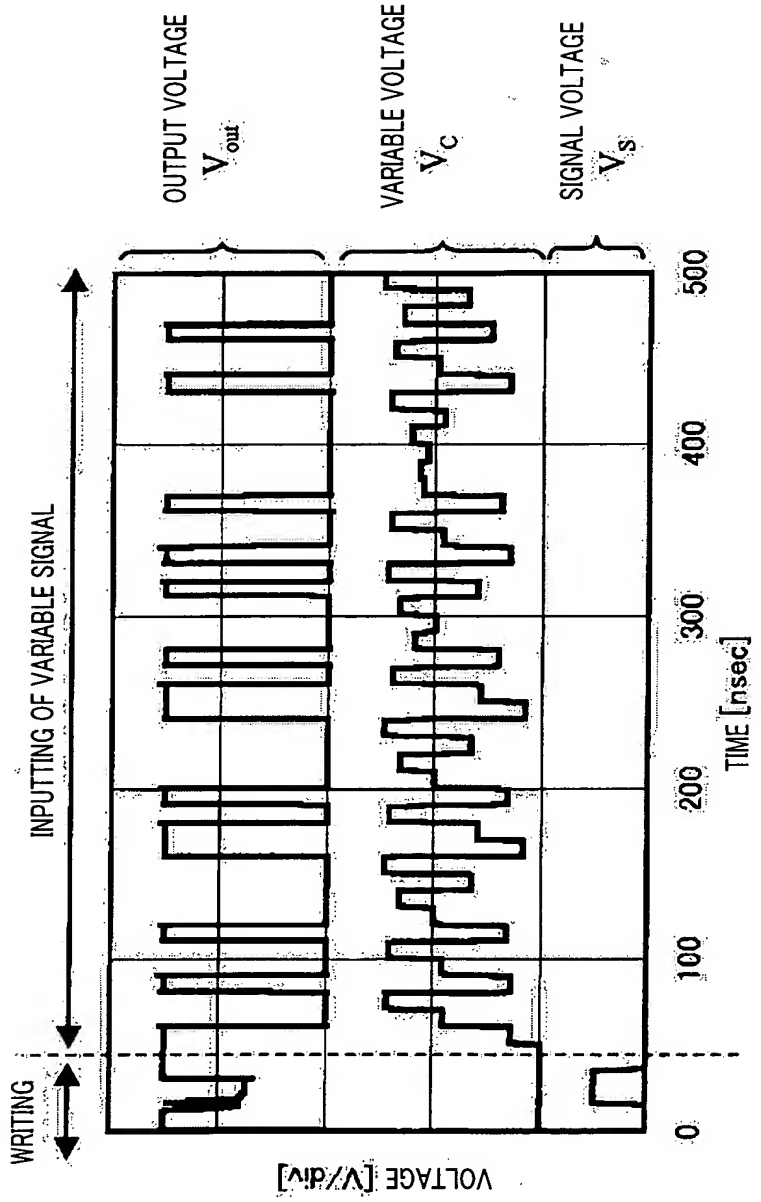

OUTPUT VOLTAGE
V_{out}
VARIABLE VOLTAGE
V_C
SIGNAL VOLTAGE
V_S
INPUTTING OF VARIABLE SIGNAL
WRITING
VOLTAGE [V/div]
TIME [nsec]
0
100
200
300
400
500

Fig. 28

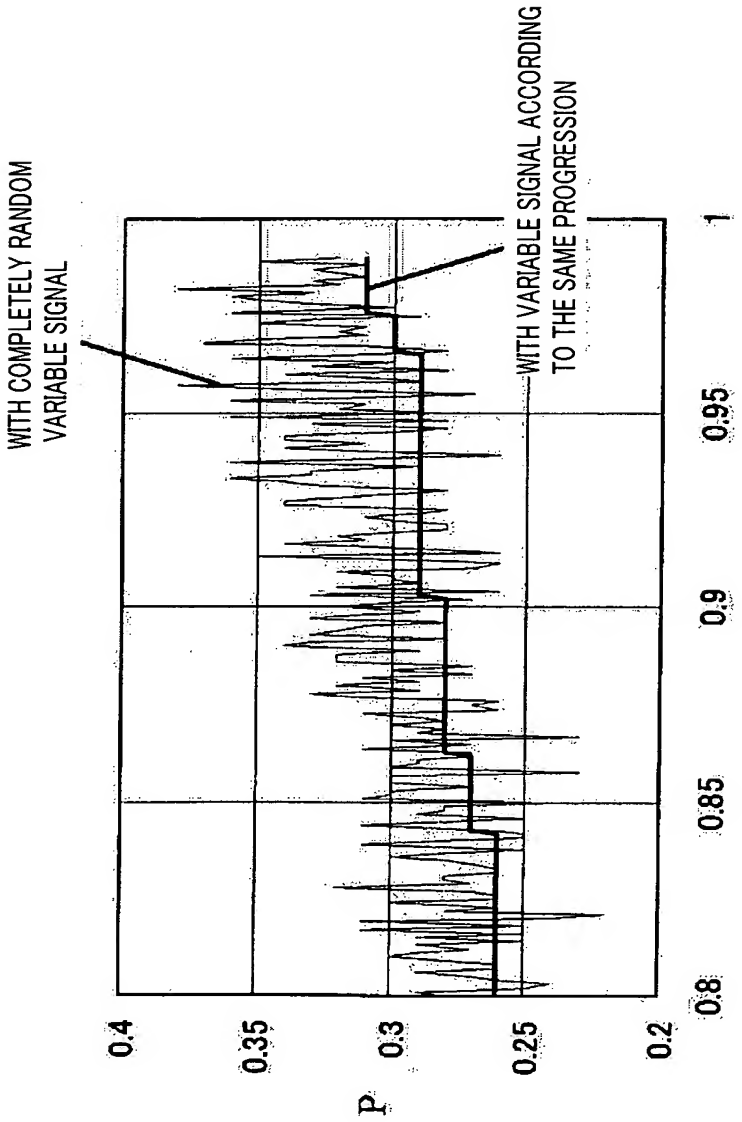

WITH COMPLETELY RANDOM VARIABLE SIGNAL
WITH VARIABLE SIGNAL ACCORDING TO THE SAME PROGRESSION
0.4
0.35
0.3
0.25
0.2
P
0.8
0.85
0.9
0.95
1
Vs

Fig. 29

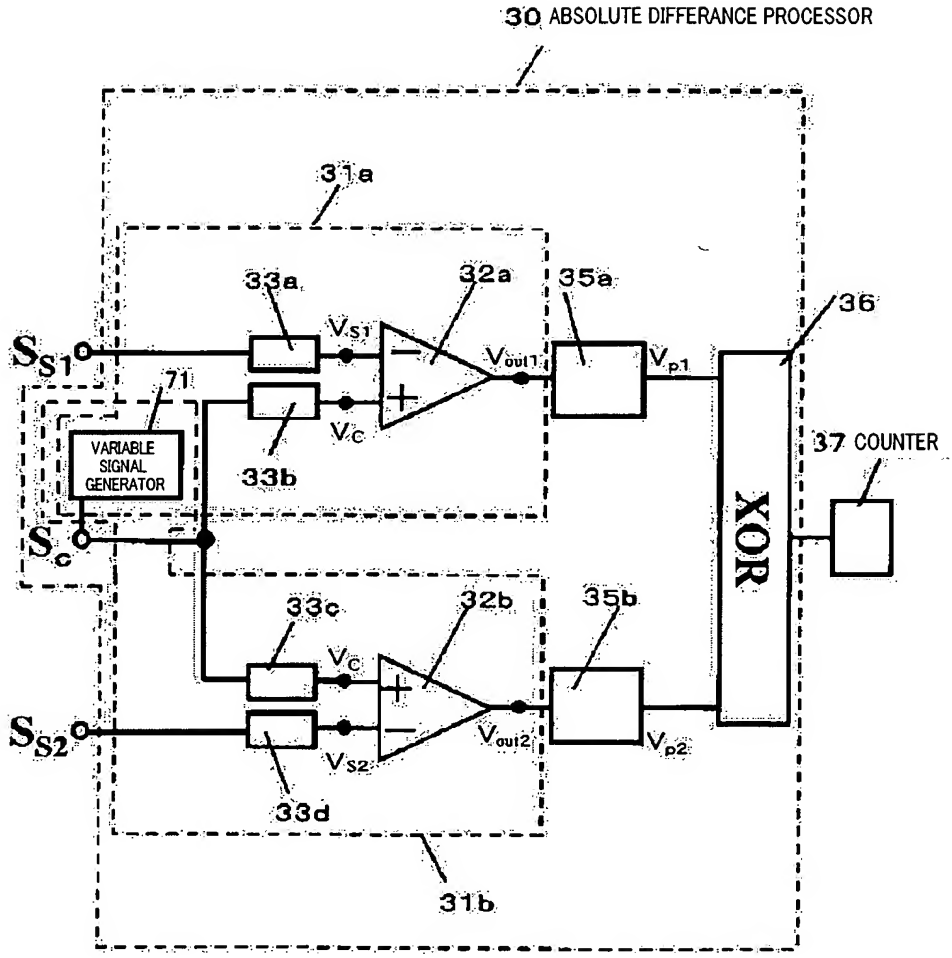

30 ABSOLUTE DIFFERANCE PROCESSOR
31a
33a
32a
35a
36
S_{S1}
V_{S1}
V_{out1}
V_{p1}
71
VARIABLE SIGNAL GENERATOR
V_C
33b
37 COUNTER
XOR
S_C
33c
32b
35b
V_C
S_{S2}
V_{out2}
V_{p2}
V_{S2}
33d
31b

Fig. 30

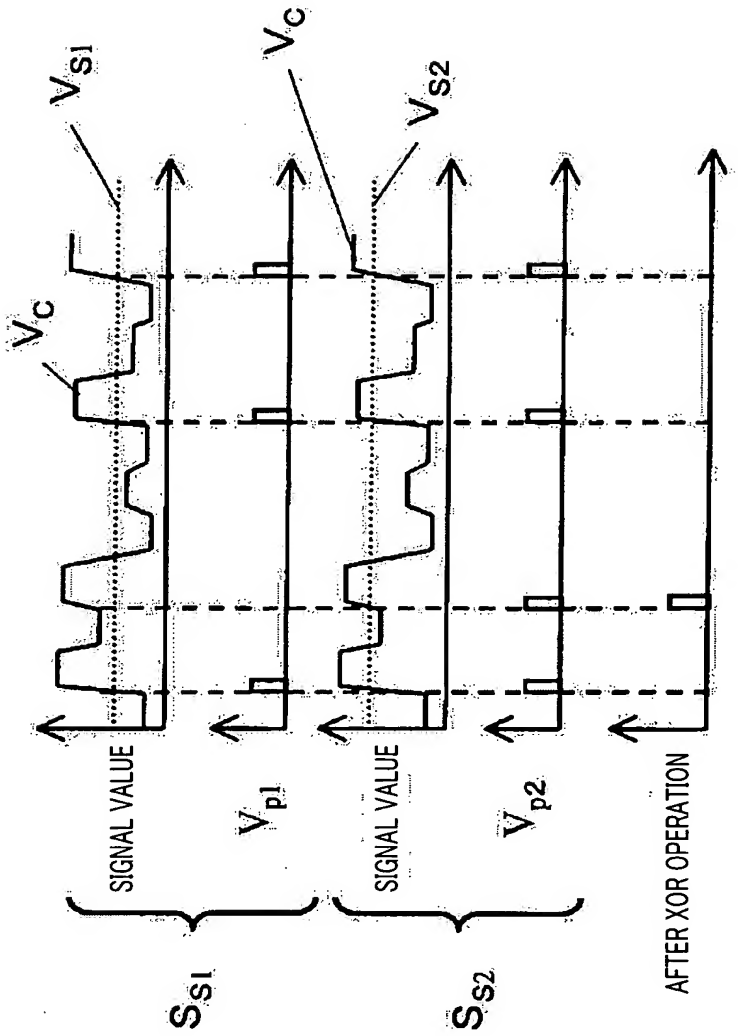

V_{S1}
V_C
V_{S2}
V_C
SIGNAL VALUE
V_{p1}
SIGNAL VALUE
V_{p2}
AFTER XOR OPERATION
S_{S1}
S_{S2}

Fig. 31

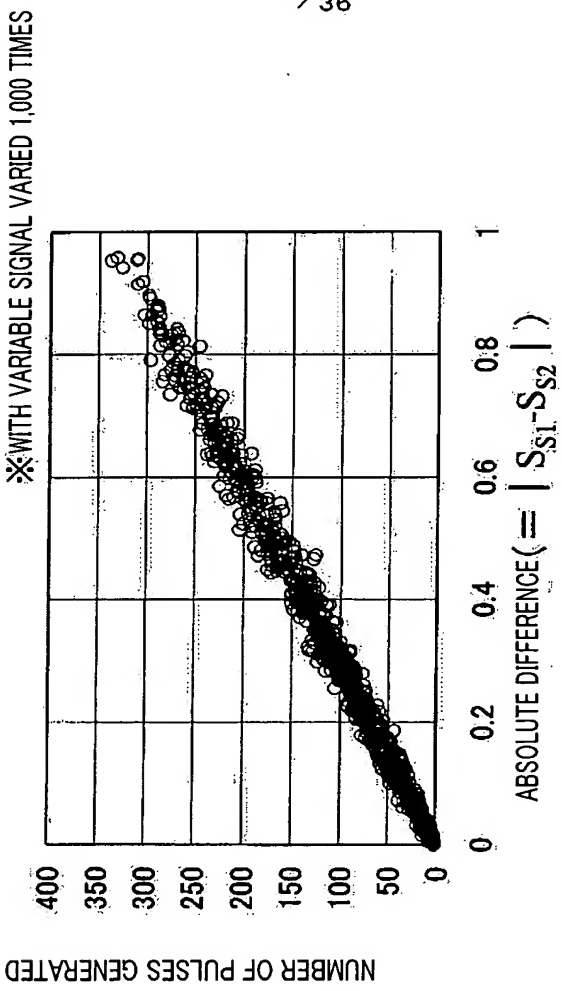

※WITH VARIABLE SIGNAL VARIED 1,000 TIMES
NUMBER OF PULSES GENERATED
400
350
300
250
200
150
100
50
0
0
0.2
0.4
0.6
0.8
1
ABSOLUTE DIFFERENCE(= | S_{S1}-S_{S2} |)

Fig. 32

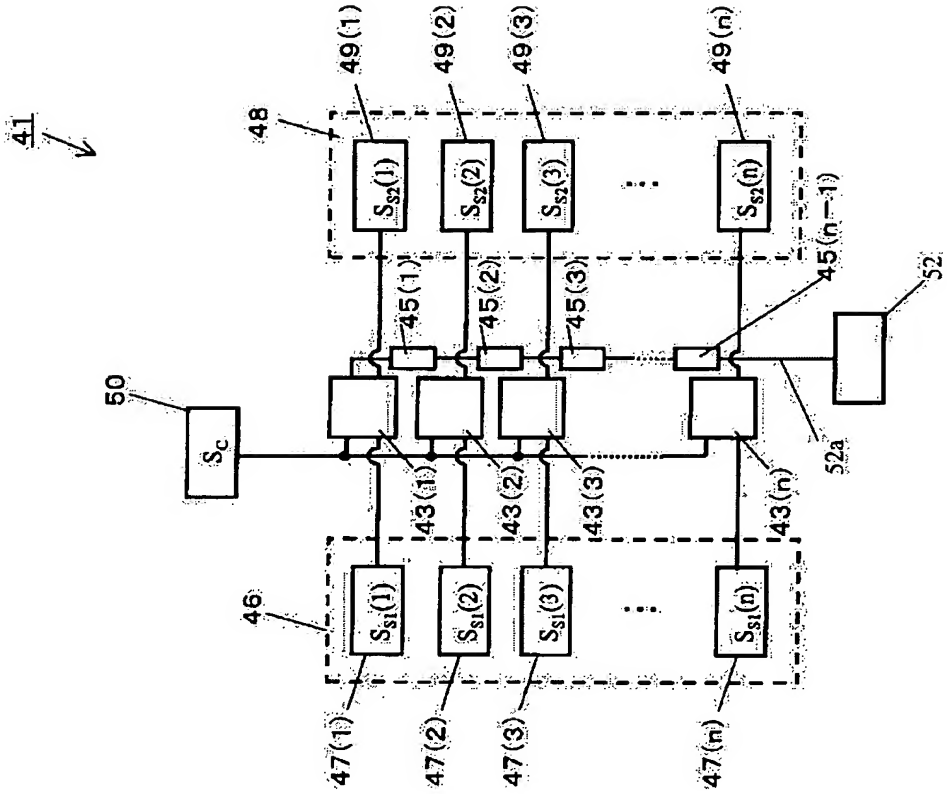

41
48
49(1)
49(2)
49(3)
49(n)
$S_{S2}(1)$
$S_{S2}(2)$
$S_{S2}(3)$
$S_{S2}(n)$
45(1)
45(2)
45(3)
45(n-1)
52
50
S_C
52a
43(1)
43(2)
43(3)
43(n)
46
$S_{S1}(1)$
$S_{S1}(2)$
$S_{S1}(3)$
$S_{S1}(n)$
47(1)
47(2)
47(3)
47(n)

Fig. 33

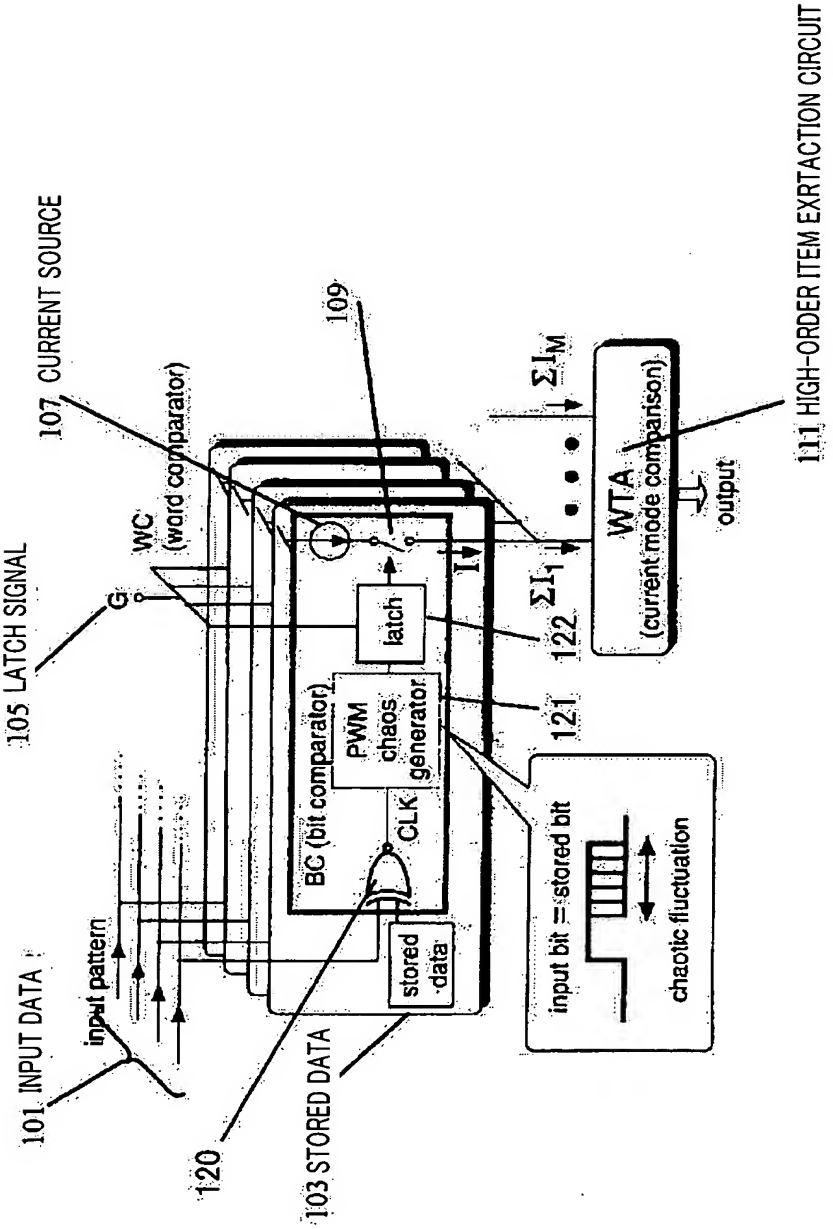

101 INPUT DATA
105 LATCH SIGNAL
107 CURRENT SOURCE
111 HIGH-ORDER ITEM EXRTACTION CIRCUIT
120
103 STORED DATA
109
WC (word comparator)
G
input pattern
BC (bit comparator)
PWM chaos generator
CLK
stored data
latch
122
121
WTA (current mode comparison)
output
input bit = stored bit
chaotic fluctuation

Fig. 34

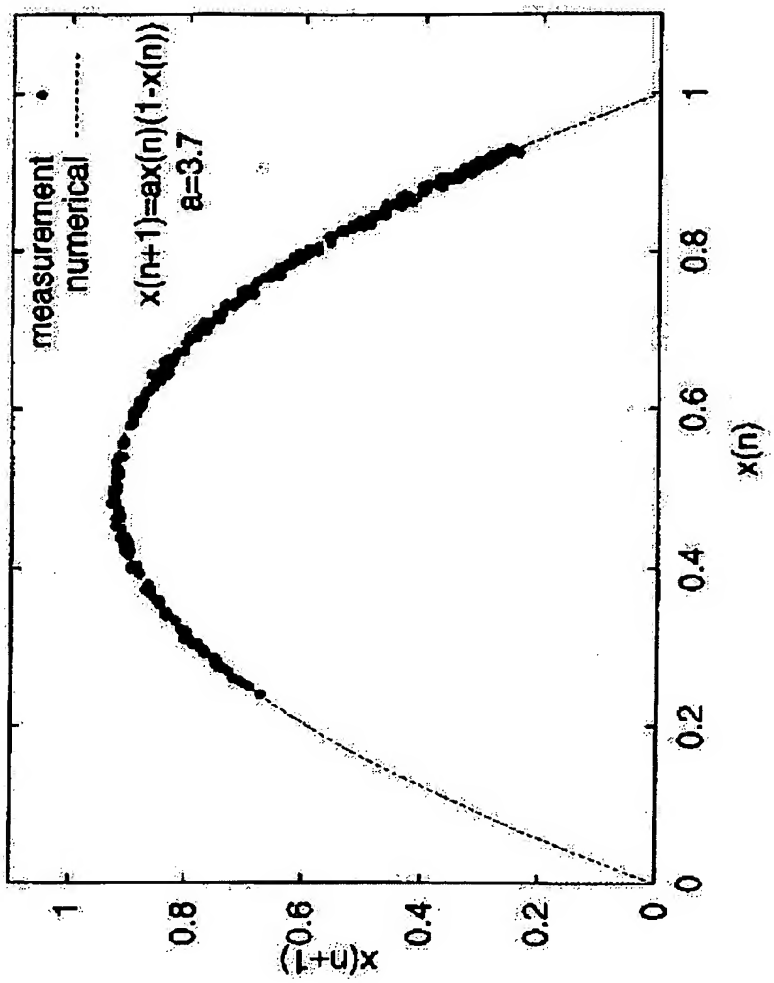


Fig. 35

LIST OF REFERENCE CHARACTERS

1 stochastic pulse generator
3 comparator
5a,5b voltage converter
7 edge detector circuit
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48 vector
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S_S input signal
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